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D Ernst, NS Kim, S Das, S Pant, R Rao, T Pham, C ... - Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual ..., 2003 - [ieeexplore.ieee.org](#)

... supply voltage is typically selected at design- time using corner **analysis**. ... Razor:

A Low-Power Pipeline Based on **Circuit-Level Timing** Speculation ...

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C Constantinescu - 2003 - [doi.ieeecomputersociety.org](#)

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MP Baze, S Buchner, WG Bartholet, TA Dao - Nuclear Science, IEEE Transactions on, 1995 - [ieeexplore.ieee.org](#)

... in much the same way that logic and **timing** simulators are ... weak points in the design,

and estimate the total **circuit static** bit **error** ... CAD **circuit** schematic 7-Y ...

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Fault list compaction through static timing analysis for efficient fault injection experiments - [all 6 versions »](#)

MS Reorda, M Violante - Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. ..., 2002 - [ieeexplore.ieee.org](#)

... SETs producing effects on the **circuit** outputs. If a more detailed **analysis** is required ...

an approach that exploits simple **static timing analysis** of combinational ...

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P Shivakumar, M Kistler, SW Keckler, D Burger, L ... - Dependable Systems and Networks, 2002. DSN 2002. Proceedings ..., 2002 - [ieeexplore.ieee.org](#)

... Section 6 discusses the implications of our **analysis** and sim ... that it does not affect

the result of the **circuit**. ... presented in this paper we use **static** NAND gates ...

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[PDF] The circuit and physical design of the POWER4 microprocessor - [all 7 versions »](#)

JD Warnock, JM Keaty, J Petrovick, JG Clabes, CJ ... - IBM Journal of Research and Development, 2002 - [csserver.evansville.edu](#)

... behind the choice of a primarily **static** design style ... effects of coupled noise on

chip **timing** and also ... Then the **circuit** design styles are discussed, including a ...

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Analysis of Single-Event Effects in Combinational Logic-Simulation of the AM2901 Bitslice Processor - [all 4 versions »](#)

LW Massengill, AE Baranski, DO Van Nort, J Meng, ... - IEEE Trans. on Nuclear Science, 2000 - [ieeexplore.ieee.org](#)

... The synthesized **circuit** contains over 1200 single-event ... among Functional Blocks Another

static analysis that can ... dynamic path **analysis** or **timing** simulation is a ...

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A 30-MHz hybrid analog/digital clock recovery circuit in 2- μ mCMOS

B Kim, DN Helman, PR Gray - Solid-State Circuits, IEEE Journal of, 1990 - [ieeexplore.ieee.org](#)

... a second-order loop with zero **static** phase error ... KIM et al.: HYBRID ANALOG/DIGITAL

CLOCK RECOVERY **CIRCUIT** ... A first-order **analysis** of thermal noise accumulation ...

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[Simulation of SEU transients in CMOS ICs - all 5 versions »](#)

N Kaul, BL Bhuva, SE Kerns - Nuclear Science, IEEE Transactions on, 1991 - [ieeexplore.ieee.org](#)
... for predicting the vulnerability of MOS **Static** RAMS (SRAMs ... 3] and a combination of
circuit-level analyses of ... 2. SEU **ANALYSIS** USING SITA Single ions intercepting ...
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[An optical analog-to-digital converter--Design and **analysis** - all 2 versions »](#)

H Taylor - Quantum Electronics, IEEE Journal of, 1979 - [ieeexplore.ieee.org](#)
... The amplified output of the rectifier **circuit** then drives the ... bit, with the exception
of a **static** phase shift. ... The **analysis** consisted of a series of simulated ...
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Fourteen ways to fool your synchronizer - all 9 versions »

R Ginosar - Asynchronous Circuits and Systems, 2003. Proceedings. Ninth ..., 2003 - ieeexplore.ieee.org

... to guarantee the **timing** of the output of the combinational **circuit**. ... **Static timing analysis** would generate setup and hold violation warnings for every signal ...

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... SETs producing effects on the **circuit** outputs. If a more detailed **analysis** is required ... an approach that exploits simple **static timing analysis** of combinational ...

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Probabilistic simulation for reliability analysis of CMOS VLSI circuits - all 7 versions »

FN Najm, R Burch, P Yang, IN Hajj - Computer-Aided Design of Integrated Circuits and Systems, ..., 1990 - ieeexplore.ieee.org

... what information about the current is needed for EM **analysis**. ... that can be applied at the **circuit** inputs during ... therefore, to use a standard **timing** simulator to ...

Cited by 130 - [Related Articles](#) - [Web Search](#)

[PS] Pattern-independent current estimation for reliability analysis of CMOS circuits - all 6 versions »

R Burch, F Najm, P Yang, D Hocevar - Annual ACM IEEE Design Automation Conference: Proceedings of ..., 1988 - eecg.utoronto.ca

... because it causes the worst **timing** delay and ... get the total expected current waveform for the **circuit**. ... For **static** signal probabilities (as opposed to probability ...

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Estimation of maximum current envelope for power bus analysis and design

S Bobba, IN Hajj - Proceedings of the 1998 international symposium on Physical ..., 1998 - portal.acm.org

... h dramatically increases the **failure rate** of interconnects ... can be obtained by performing a **static timing analysis**. ... controlled syn-chronous **circuit** switch at ...

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Impact of deep submicron technology on dependability of VLSI circuits - all 8 versions »

C Constantinescu - Dependable Systems and Networks, 2002. Proceedings. ..., 2002 - ieeexplore.ieee.org

... faults for CMOS microprocessors and **static** and dynamic ... **analysis** showed that a VLSI **circuit** experienced clock ... These **timing** violations were responsible for multi ...

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Method for evaluating the timing of digital machines with statistical variability in their delays - all 3 versions »

WE Donath, RB Hitchcock, JP Soreff - US Patent 5,365,463, 1994 - freepatentsonline.com

... delay spreads peculiar to each **circuit** type ... A further **analysis** is then required to find ... specifications only provide improvement over **static timing** techniques at ...

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RAPPID: An asynchronous instruction length decoder - all 19 versions »

S Rotem, K Stevens, R Ginosar, P Beerel, C Myers, ... - Proc. International Symposium on Advanced Research in ..., 1999 - doi.ieeecs.org
... self-timed circuits using any future **circuit** or implementation ... The design uses **static**
and domino gates from ... to noise on control lines, **timing** verification, and ...
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[Statistical analysis of timing rules for high-speed synchronousVLSI systems - all 4 versions »](#)

CS Li, KN Sivarajan, DG Messerschmitt, IBMTJWR ... - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1999 - ieeexplore.ieee.org
... environment in which there is no **circuit** noise or ... 1) Conventional Pipelining: In
this scheme, the **timing** constraint in ... to T 0 t setup **static** ;j ; **static** ...
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Performance and Reliability Verification of C6201/C6701 Digital ...

most unique hold **time violations** yet Max-R **corner** produced. some unique **violations** that ... **static timing analysis** eliminated a number of false paths due to ...

doi.ieeecomputersociety.org/10.1109/ICCD.1999.808591 - [Similar pages](#)

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ASIC-System On Chip (SoC)-VLSI Design: Process-Voltage-Temperature ...

Process-Voltage-Temperature (PVT) Variations and **Static Timing Analysis** ... at least as fast as predicted and will not suffer from hold-**time violations**. ...

asic-soc.blogspot.com/2008/03/process-variations-and-static-timing.html - 108k - [Cached](#) - [Similar pages](#)

Voltage-Aware Static Timing Analysis

Abstract—**Static timing analysis** (STA) techniques allow a de- signer to check the **timing** of a circuit at different process **corners**, ...

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Timing window applications in ultrasparc-iii tm microprocessor ...

Max Edge - Switching **Time**. Min Edge - Switching **Time**. **Timing Window File**. **Static Timing Analysis**. Noise **Violation List**. Noise **Analysis Results** ...

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Printed Circuit Design & Fab - Timing Analysis Principles for ...

In **static timing analysis**11, signal paths are ascertained by tracing the design ... and detect several types of **timing violations** including setup and hold, ...

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May 4, 2008 ... variations increases, **corner**-based **static timing analysis** (STA) ... verification and to precisely determine **timing violations**, the ...

atrak.usc.edu/~massoud/Papers/stat-CSHT-characterization-glsvlsi08.pdf - [Similar pages](#)

Method and apparatus for the analysis and optimization of ...

After **timing analysis**, the design can be queried for worst **timing violations** or other performance data. A query could be for a specific **corner**/mode ...

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Reliability Issues in Deep Deep Submicron Technologies: Time ...

manner. **Static timing analysis** (STA) which computes the critical **path** delays ... since no synchronization boundaries exist to create **timing violations**. ...

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place:. (i) The original mapped netlist is placed on the FPGA device. (ii) **Static timing analysis** is performed on the placed circuit. The longest **path** delay ...

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EETimes.com - Variability upends designers' plans

"Exhaustive **corner** analysis is **exhausting**," said Chandu Visweswariah, ... transition from gate-level **timing simulation** to **static timing** analysis before it. ...

www.eetimes.com/showArticle.jhtml?articleID=174301075 - 54k - [Cached](#) - [Similar pages](#)

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static timing analysis of the design and dynamic **timing. simulation** patterns and 3 **simulation corners** on an average for each. type of pattern. ...

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A Framework for Distributed and Hierarchical Design-For-Test

timing simulation. The design team integrates the tools into a circuit blocks, the effort involved in **static timing** analysis can be ...

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On Power-profiling and Pattern Generation for Power-safe Scan Tests

lumped gate delay **model** is used for performing **timing**-based hazard. analysis. The earliest and the latest expected signal arrival times, obtained by **Static** ...

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DeepChip: ESNUG Post 0322: > John, I was looking through some of ...

It is actually a pretty powerful **static timing** analyser that doesn't need mechanism - Automatic generation of **simulation model** together with a ready ...

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The **simulation** consists of an initialisation phase, where **static** patch data ... fuel in a patch is **exhausted** and no further burning events occur for that ...

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DAC'98 Abstracts

As functional failures due to noise really a problem in a **static** CMOS design ? Session 28: Interconnect Modeling and **Timing Simulation** ...

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12000 inspections per year using Acceleration **Simulation Mode** (ASM) test equipment. ... count until the total vehicle population is **exhausted**. ...

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Context-sensitive constraint driven uniquification and ...

The method of claim 5, wherein said constraint for **timing** of said cell comprises circuit topology, **model** extraction technology, transistor **simulation** ...

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